IN THE CLAIMS:

The status of all the claims of the application is presented below:

1. **(Currently Amended)** A method of routing packets between a plurality of circuit within a node of a network ~~in a system~~, comprising:

~~receiving~~ examining a ~~packet~~ ~~plurality of packets~~, ~~each~~ the packet including [[a]] an internal routing label specifying one of a plurality of circuit cards and a packet type;

routing ~~each~~ the packet to ~~a destination within the system~~ the one of the plurality of circuit cards specified in the internal routing label in response to the packet type being indicative of a ~~first type. data packet; and~~

~~routing each packet to a processor within the system and sending a reply packet to a sender specified in the routing label in response to the packet type being indicative of a control packet.~~

2. **(Currently Amended)** The method, as set forth in claim 1, wherein routing ~~each~~ the packet to ~~a destination~~ the one of the plurality of circuit cards comprises routing each packet to ~~the destination specified~~ by at least a shelf and slot numbers ~~of the destination~~ included in the internal routing label.

3. **(Currently Amended)** The method, as set forth in claim 1, wherein routing ~~each~~ the packet to ~~a destination~~ the one of the plurality of circuit cards comprises routing each packet ~~to the destination specified by~~ based on a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label ~~for transporting the packet~~.

4. **(Currently Amended)** The method, as set forth in claim 1, wherein sending the reply packet to a sender comprises routing the reply packet to the ~~sender specified by~~ one of the plurality of circuit cards based on shelf and slot numbers ~~of the sender~~ included in the routing label.

5. **(Currently Amended)** The method, as set forth in claim 32 ~~1~~, wherein sending the reply packet to ~~a sender~~ the one of a plurality of circuit cards comprises routing the reply packet ~~to the sender specified by~~ based on a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label for transporting the reply packet.

6. **(Currently Amended)** The method, as set forth in claim 1, wherein routing ~~each~~ the packet to ~~a destination~~ the one of a plurality of circuit cards comprises:

receiving ~~each~~ the packet at a switch; and

switching ~~each~~ the packet to the one of a plurality of circuit cards ~~destination~~ coupled to a predetermined port of the switch as specified by shelf and slot numbers of the destination included in the internal routing label.

7. **(Currently Amended)** The method, as set forth in claim 1, wherein routing ~~each~~ the packet to ~~a destination~~ the one of a plurality of circuit cards comprises:

receiving ~~each~~ the packet at a switch; and

routing ~~each~~ the packet to the one of a plurality of circuit cards ~~destination~~ coupled to a predetermined port of the switch as specified by a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label ~~for transporting the packet~~.

8. **(Currently Amended)** The method, as set forth in claim 32 ~~1~~, wherein routing ~~each~~ the packet to a processor and sending the reply packet ~~to a sender~~ comprises:

receiving ~~each~~ the packet at a switch;

switching the packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet to the ~~sender~~ one of the plurality of circuit cards coupled to a second predetermined port of the switch specified by shelf and slot numbers ~~of the sender~~ included in the internal routing label.

9. **(Currently Amended)** The method, as set forth in claim 32 ~~1~~, wherein routing each packet to a processor and sending the reply packet to a sender comprises:

receiving each packet at a switch;

switching the packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet to the ~~sender~~ one of the plurality of the circuit cards coupled to a second predetermined port of the switch specified by a shelf identifier, a slot identifier, a link identifier, and a channel identifier included in the internal routing label for transporting the reply packet.

10 -11. **(Cancelled)**

12. **(Currently amended)** The method, as set forth in claim 1 ~~11~~, further comprising popping the internal routing label ~~from onto the~~ a label ~~information table~~ stack on the packet after receiving the packet at the one of the plurality of circuit cards. ~~destination within the system.~~

13. **(Currently amended)** The method, as set forth in claim 32 ~~11~~, further comprising popping the routing label from the label information table stack after receiving the packet at the processor within the system.

14-22. **(Cancelled)**

23. **(Currently Amended)** The method, as set forth in claim [[22]] 1, further comprising pushing the internal routing label onto a label ~~information table~~ stack of the packet after receiving the packet.

24. **(Currently Amended)** The method, as set forth in claim [[23]] 1, further comprising:

~~accessing the routing label in the label information table stack; and~~

popping the internal routing label from ~~the~~ a label ~~information table~~ stack of the packet after receiving the packet at the one of a plurality of circuit cards ~~destination~~ within the node ~~system~~.

25. **(Currently Amended)** The method, as set forth in claim 23, further comprising popping the routing label from the label ~~information table~~ stack after receiving the packet at the processor within the node ~~system~~.

26 – 27. **(Cancelled)**

28. **(Currently Amended)** The method, as set forth in claim [[22]] 23, wherein routing [[a]] ~~the~~ packet to ~~a destination~~ the one of the plurality of circuit cards comprises:

receiving the packet at a switch; and

switching the packet to the ~~destination~~ one of the plurality of circuit cards coupled to a predetermined port of the switch coupled to the one of the plurality of circuit cards specified ~~as specified by the shelf, slot and link identifiers of the destination included~~ in the routing label.

29. **(Currently Amended)** The method, as set forth in claim [[22]] 23, wherein routing [[a]] ~~the~~ packet to the one of the plurality of circuit cards to ~~a destination~~ comprises:

receiving the packet at a switch; and

switching the packet to the ~~destination~~ one of the plurality of circuit cards coupled to a predetermined port of the switch as specified by ~~the~~ at least a shelf identifier[[,]] and slot identifier, ~~link identifier, and a channel identifier~~ included in the routing label for transporting the packet.

30. **(Currently Amended)** The method, as set forth in claim [[22]] 23, wherein routing [[a]] ~~the~~ packet to a processor and sending the reply packet ~~to a sender~~ comprises:

receiving the packet at a switch;

switching the packet to a predetermined port of the switch coupled to the processor; and

switching the reply packet to the ~~sender~~ one of the plurality of circuit cards coupled to a second predetermined port of the switch specified by at least a ~~the~~ shelf[[,]] and slot ~~and link~~ identifiers ~~of the sender~~ included in the internal routing label.

31. **(Cancelled)**

32. **(New)** The method of claim 1, further comprising routing the packet to a processor within the system and sending a reply packet to the one of the plurality of circuit cards specified in the internal routing label in response to the packet type being indicative of a control packet.

33. **(New)** Apparatus at a node of a network, comprising:

a plurality of circuit cards and a switching fabric;

means for routing a packet through the switching fabric to one of the plurality of circuit cards based on an internal routing label attached to the packet; and

means for removing the internal routing label prior to transmission of the packet from the apparatus.

34. **(New)** The apparatus of claim 33, further comprising:

a processor,

the processor including means for sending a reply packet in response to receiving a control packet to one of the plurality of circuit cards identified in the internal routing label.

35. **(New)** The node of claim 34, wherein the internal routing label further includes a packet type identifier.

36. **(New)** The apparatus of claim 35 wherein the means for routing also routes based, at least in part, on the packet type identifier.

37. **(New)** The apparatus of claim 35, wherein the means for routing includes means for routing the packet to the processor if the packet type identifier indicates a control packet type.

38. **(New)** The apparatus of claim 33, wherein the internal routing label includes at least one field for identifying the location of one of the plurality of the circuit cards within the node.

39 **(New)** The apparatus of claim 38, wherein the at least one field for identifying the location of one of the plurality of circuit cards within the node includes identifiers for a shelf and a slot of the one of the plurality of circuit cards.